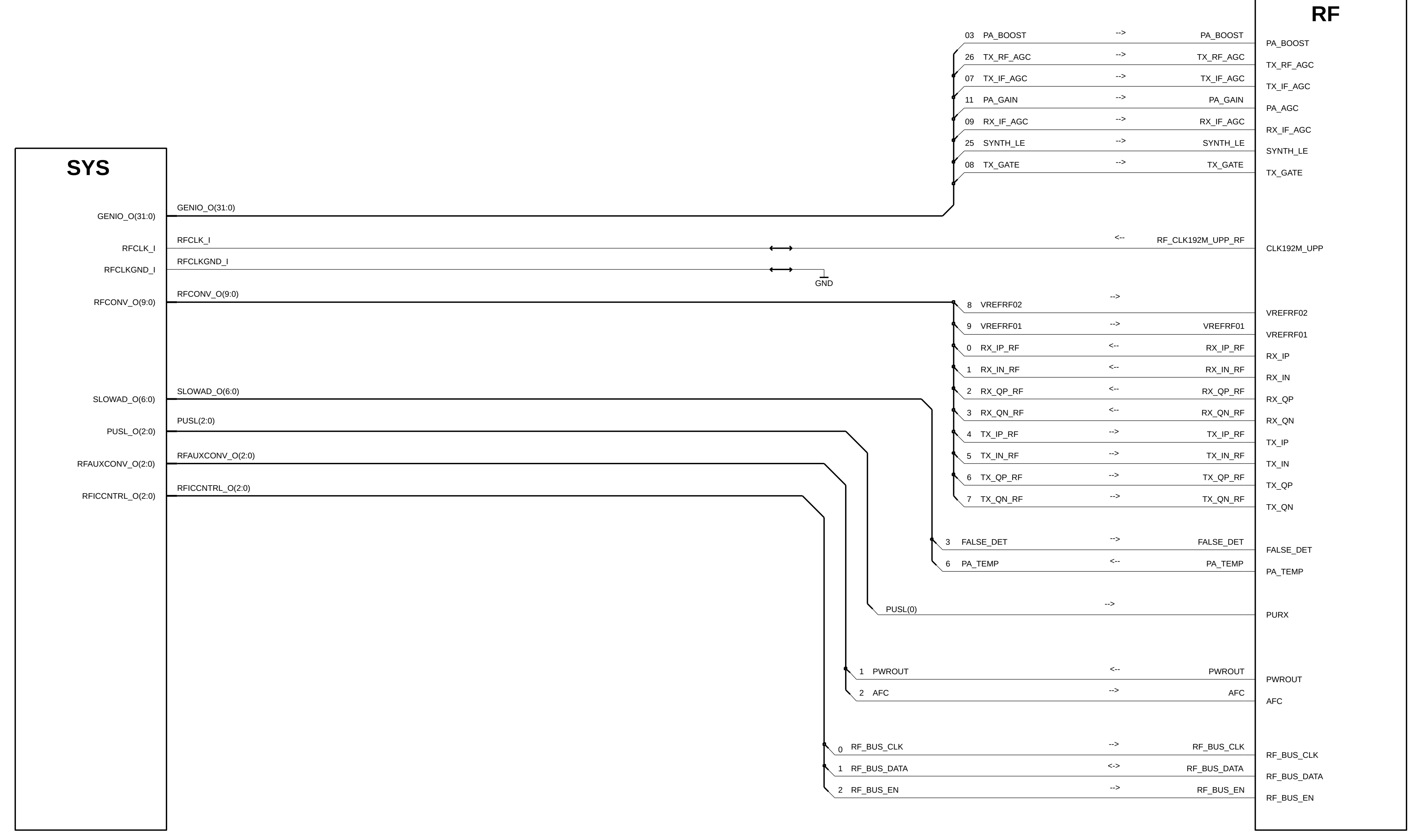
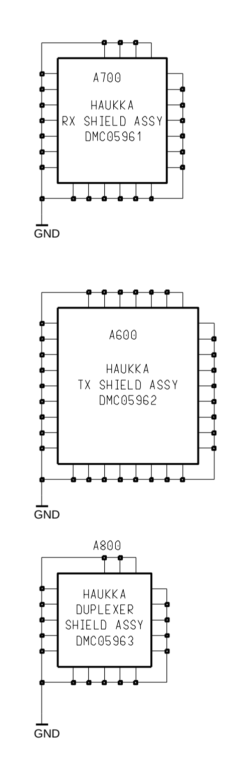
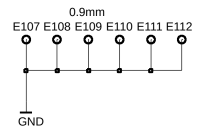
RF/BB

REVISION	CR NUMBER INCORPORATED	DATE COMPLETED
1AK_01	PROTOTYPE RELEASE (B1.0)	16-JUL-2002
1AK_02	PROTOTYPE RELEASE (B2.0)	16-SEP-2002
1AK_03	69052 69143 69172 69282 69370 69376 69379 69383 69385 69464 69466 69467 69572 69573 69574 69575 69576 69577 69624 69830 69834 70090	21-NOV-2002
1AK_04	70278 70595 70612 70892 70893 70894 70950 70951 70955 70957	17-DEC-2002
1AK_05	71415 71509 71696 71927	09-JAN-2003
1AK_06	72827	30-JAN-2003
1AK_06.1	73498	12-FEB-2003 IKKIM
1AK_06.2	73685	18-FEB-2003 IKKIM
1AK_06.3	74631	6-MAR-2003 IKKIM
1AK_07	74778 75084 75167 75463	19-MAR-2003 IKKIM

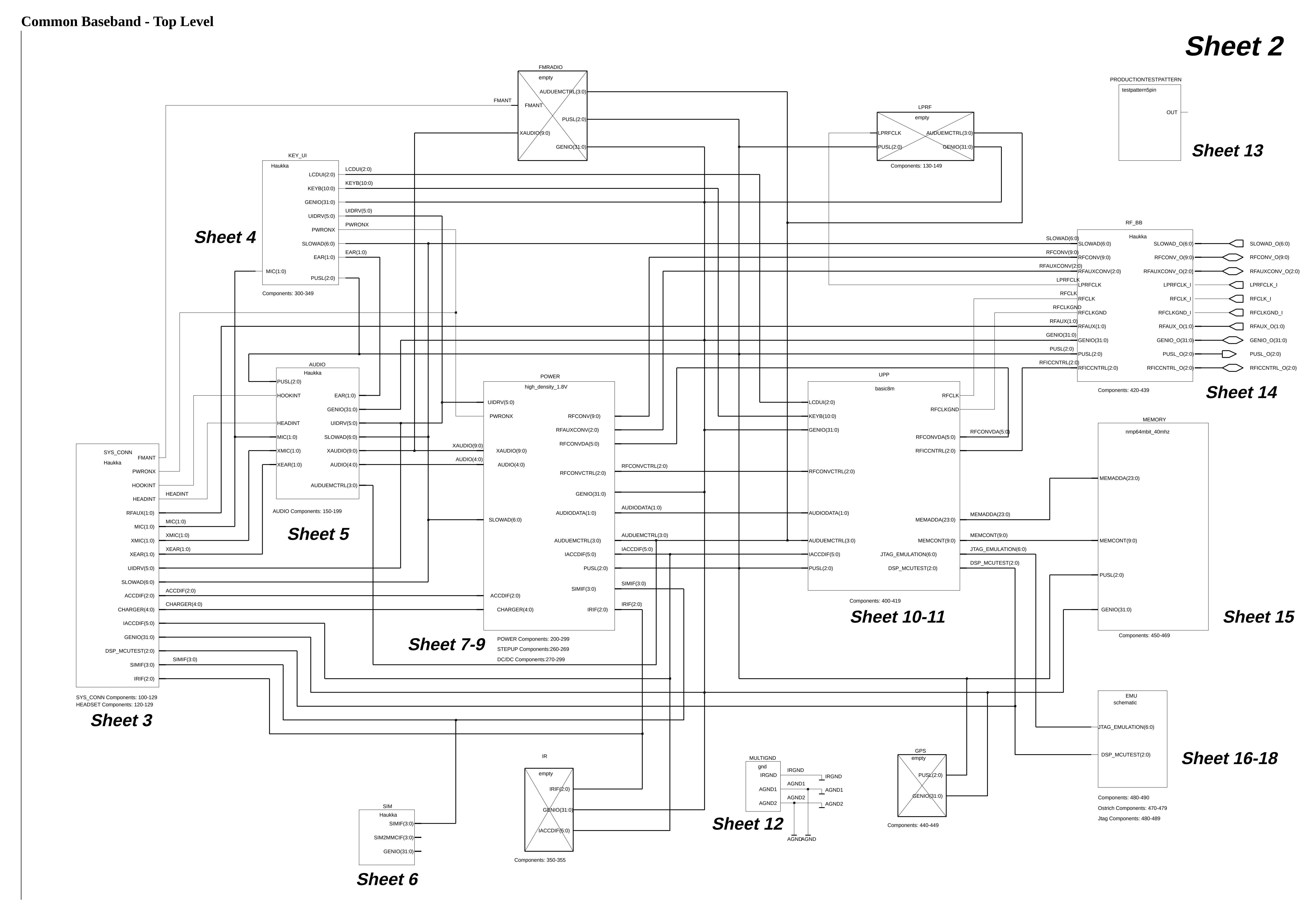


RF SHIELDS

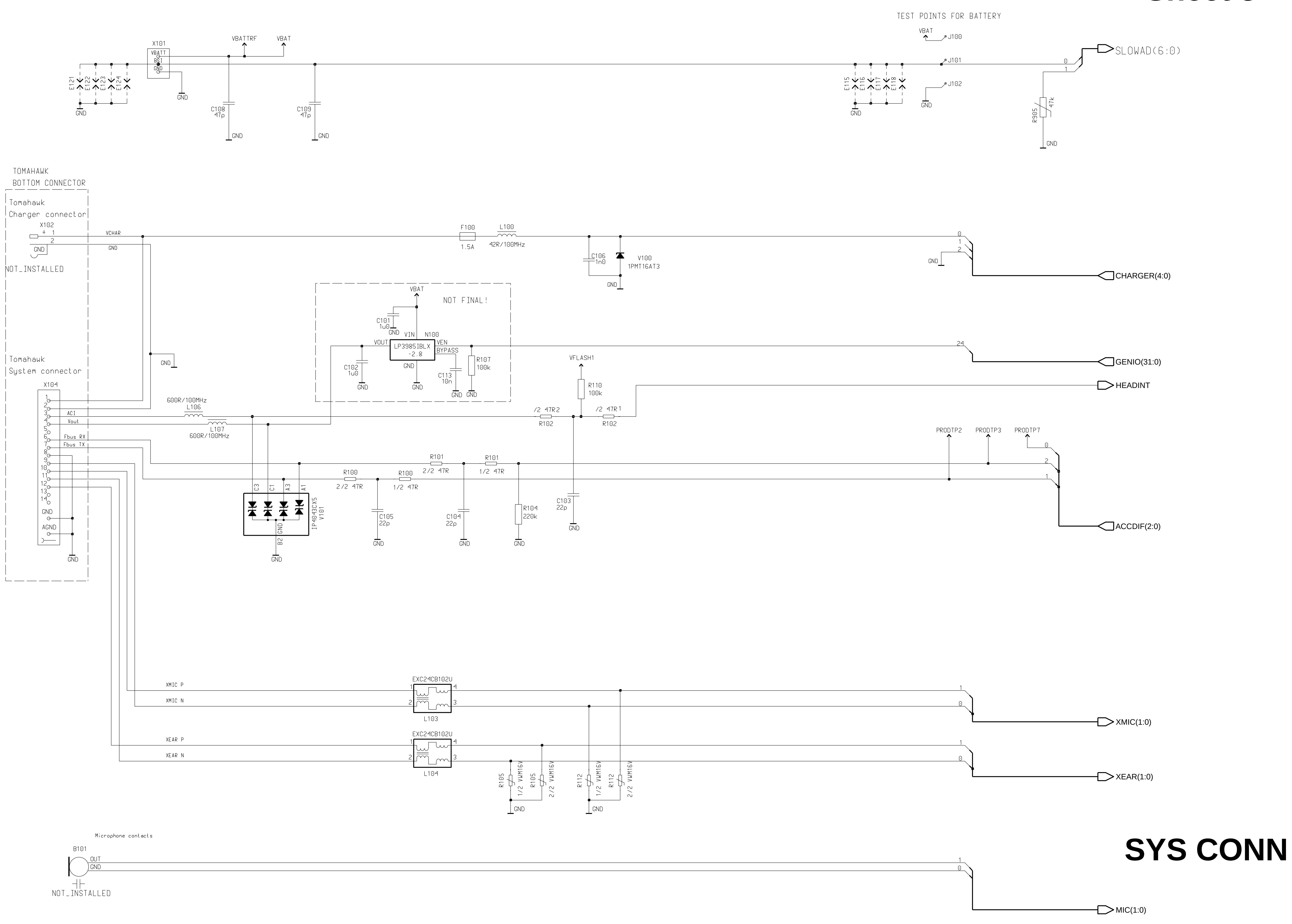




Common Baseband - Top Level

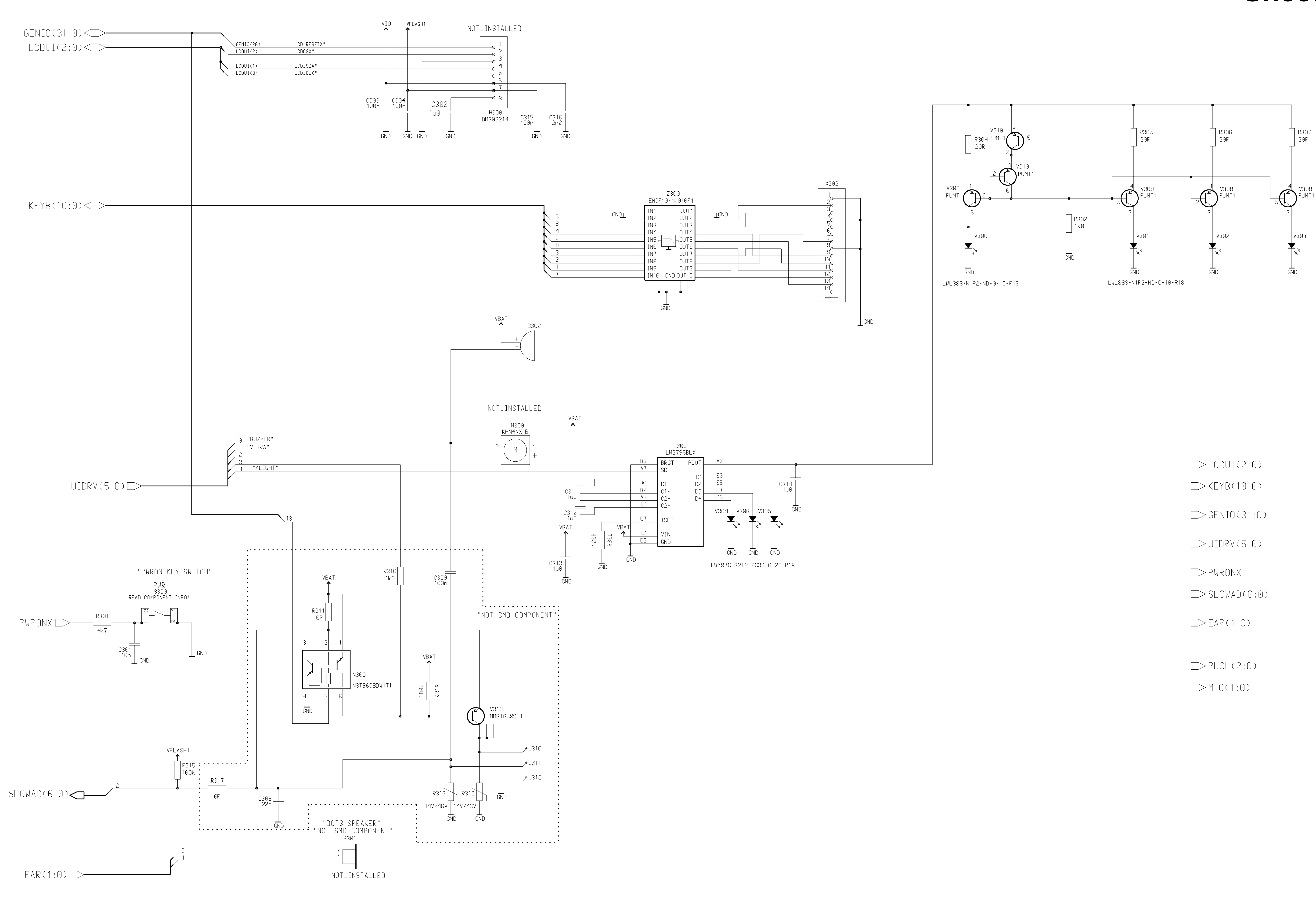


System Connector

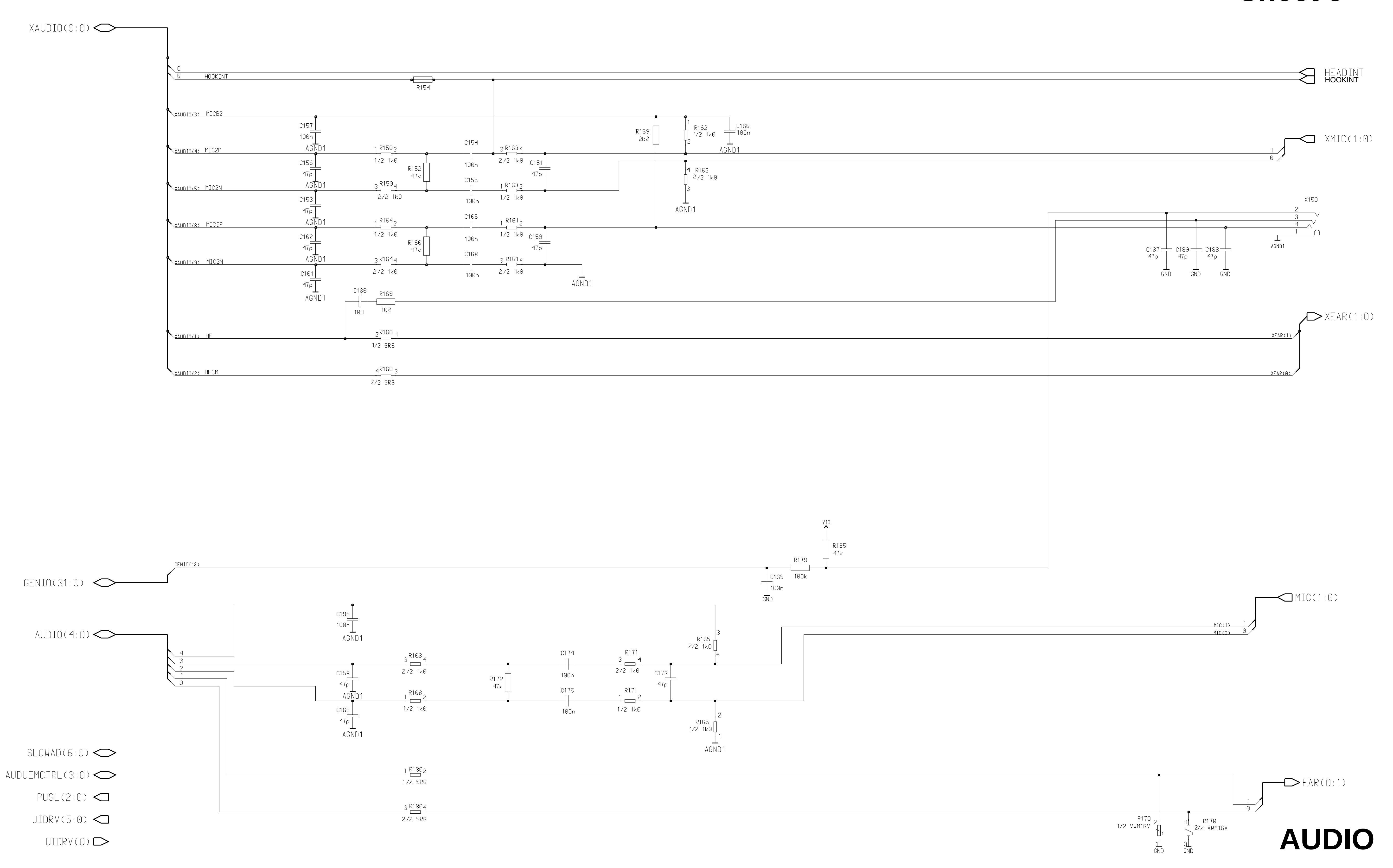


User Interface

Sheet 4

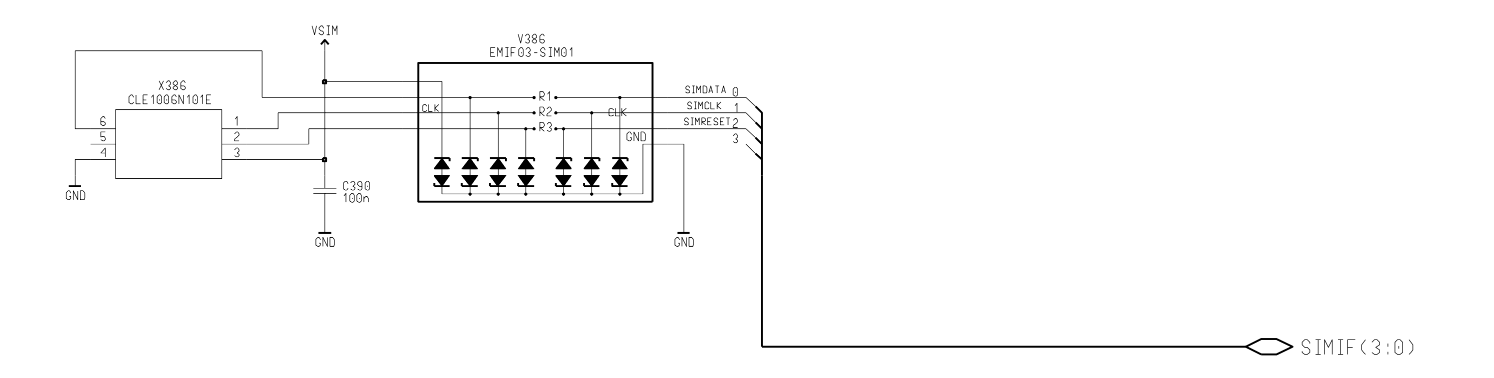


Audio


Sheet 5
XAUDIO(9:0)
HEADINT
HOOKINT
XMIC(1:0)
X150
XEAR(1:0)
GENIO(31:0)
AUDIO(4:0)
MIC(1:0)
SLOWAD(6:0)
AUDUEMCTRL(3:0)
PUSL(2:0)
UIDRV(5:0)
UIDRV(0)
EAR(0:1)
AUDIO

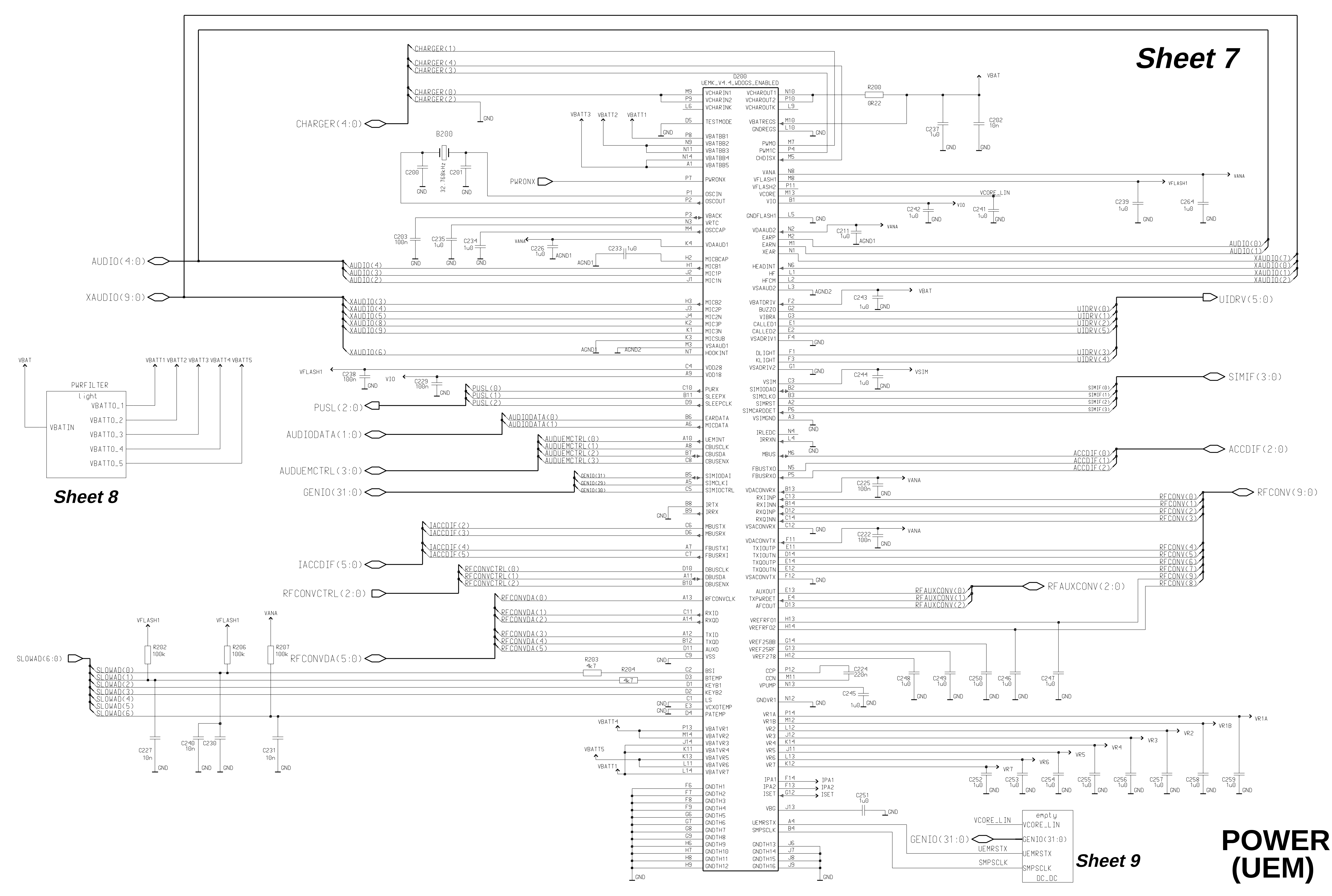
SIM Reader

Sheet 6



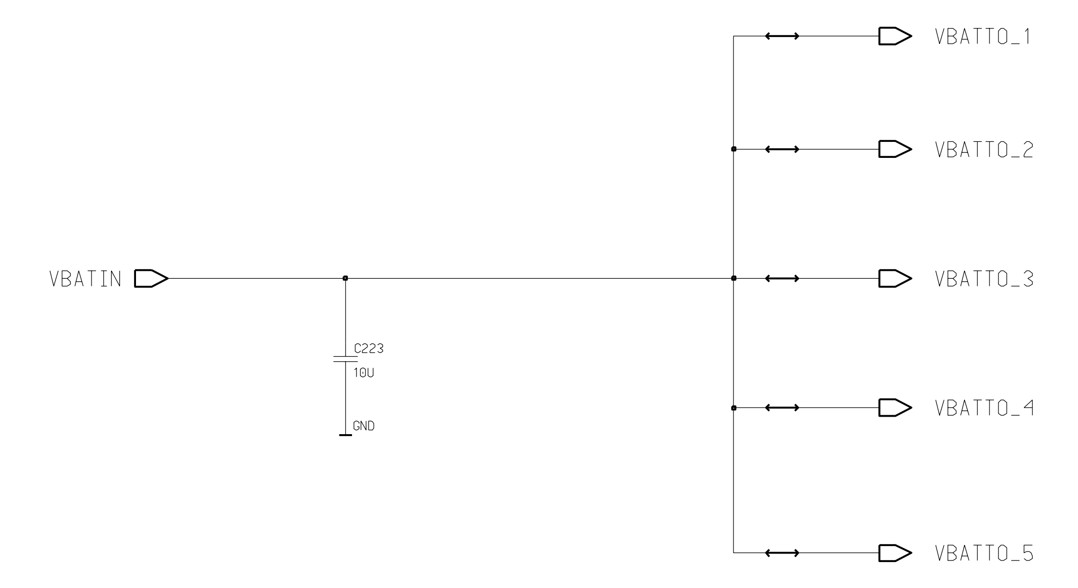
SIM

UEM


Sheet 7
Sheet 8
Sheet 9
POWER
(UEM)
CHARGER(4:0)
AUDIO(4:0)
XAUDIO(9:0)
PUSL(2:0)
AUDIODATA(1:0)
AUDUEMCTRL(3:0)
GENIO(31:0)
IACCDIF(5:0)
RFCONVCTRL(2:0)
RFCONVDA(5:0)
SLOWAD(6:0)
UIDRV(5:0)
SIMIF(3:0)
ACCDIF(2:0)
RFCONV(9:0)
RFAUXCONV(2:0)
PWRONX
PWRFILTER
D200
UEMK_V4.4_WDOGS_ENABLED
B200
32.768kHz
R200
0R22
VBAT
VANA
VFLASH1
VIO
VCORE_LIN
UEMRSTX
SMPSCLK
DC_DC

Power Filter

Sheet 8



POWER FILTER

DC/DC Converter

Sheet 9

VCORE_LIN

VCORE

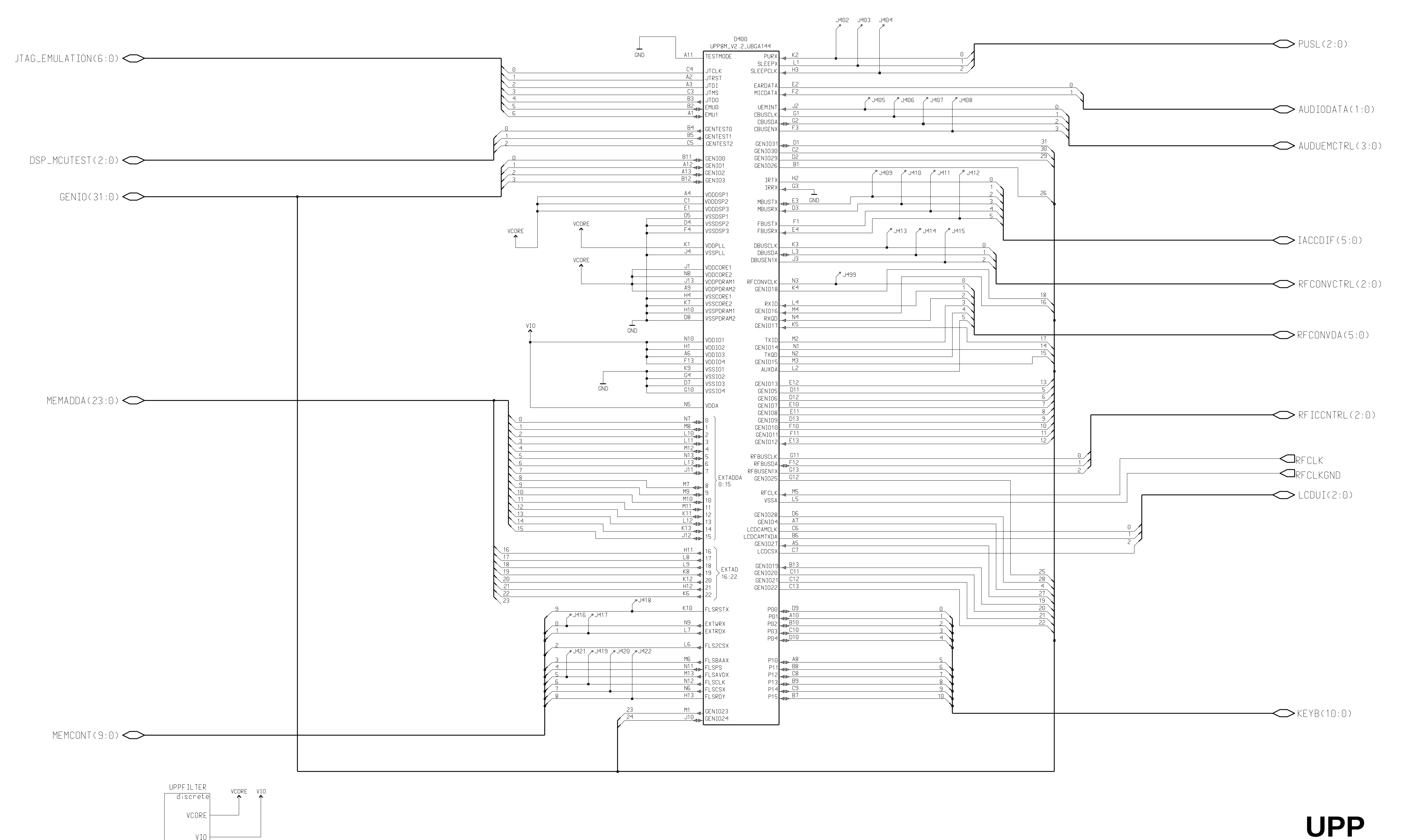
GENIO(31:0)

UEMRSTX

SMPSCLK

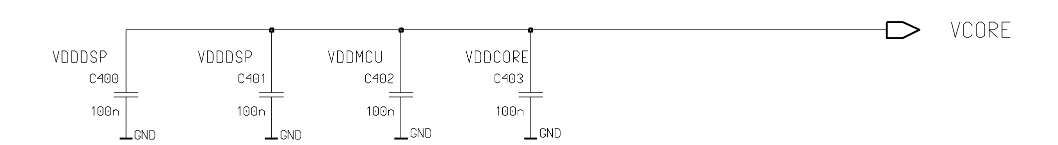
DC/DC CONVERTER

UPP 8M Implementation

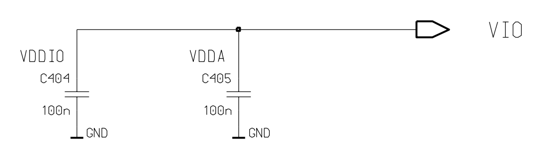


UPP Filter

Sheet 11



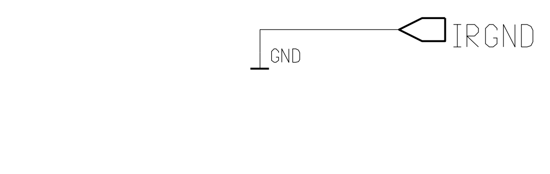
Place caps near UPP

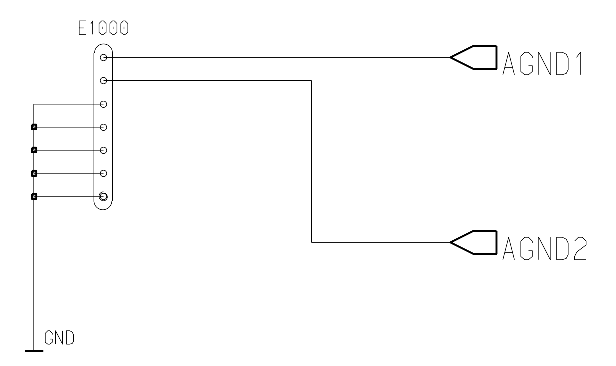


UPP_FILTER

MultiGND

Sheet 12

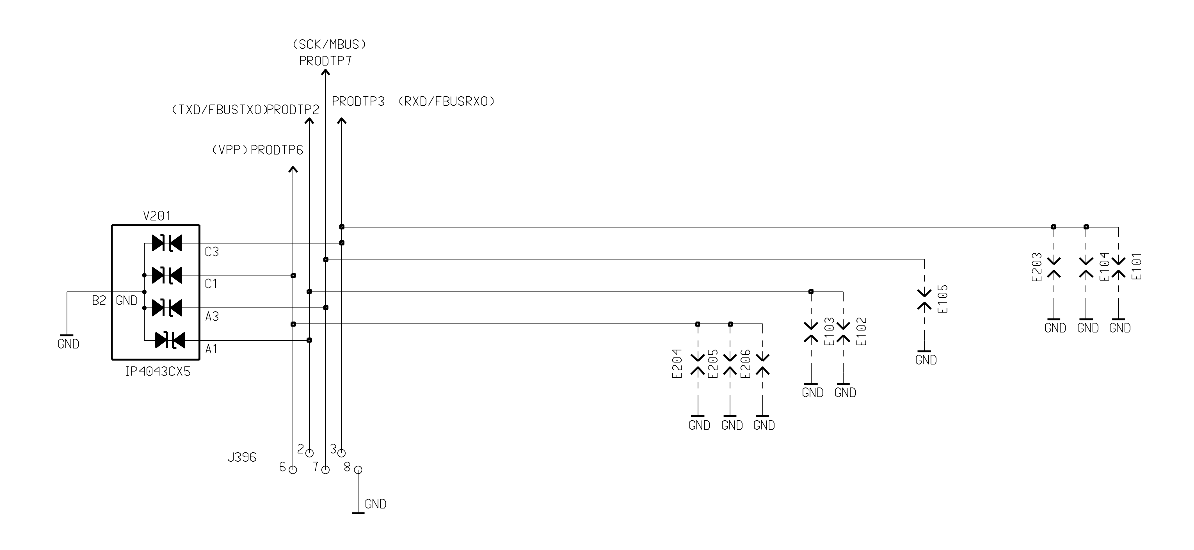




MULIT GND

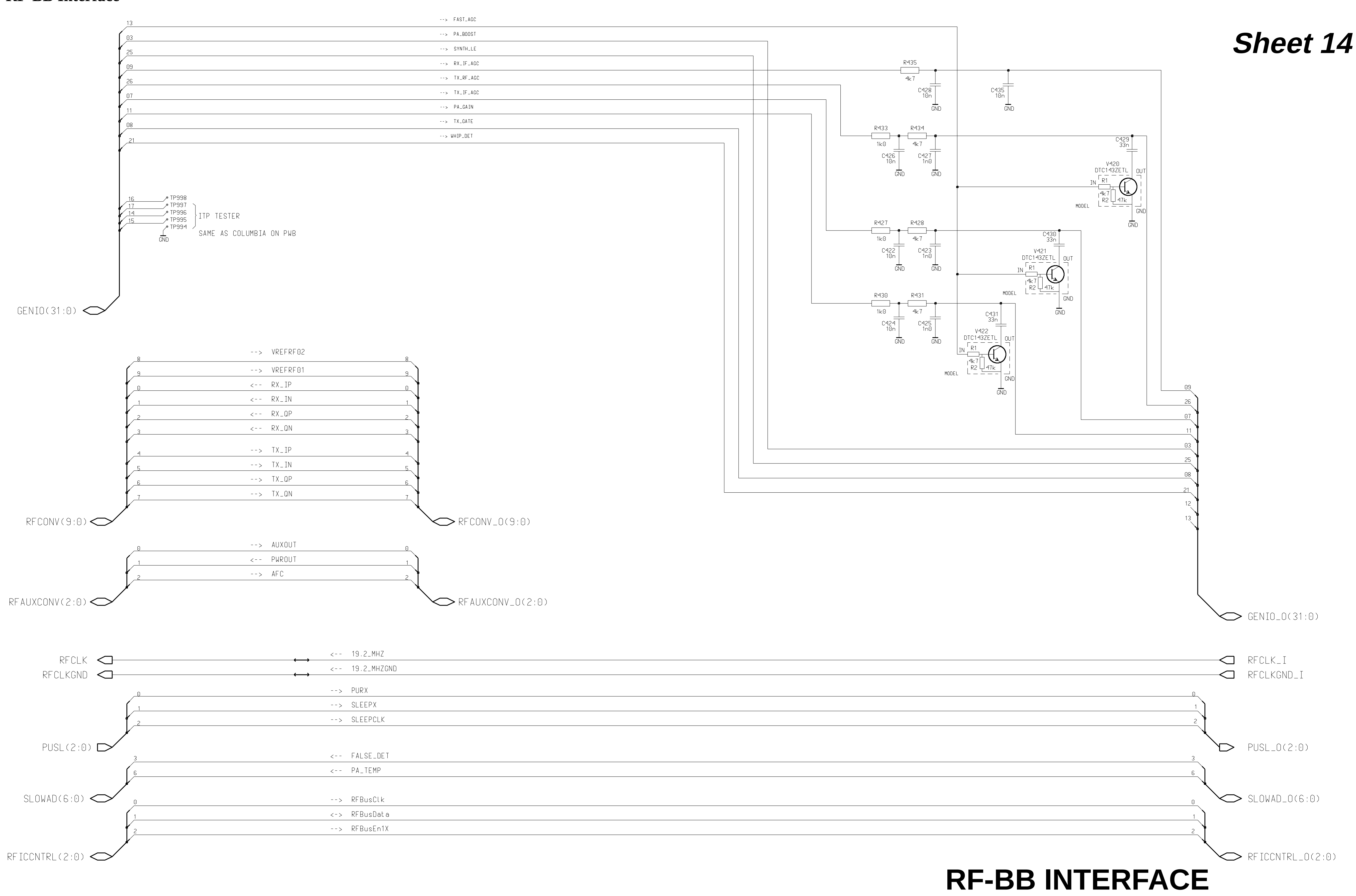
5-pin Production Test Pattern

Sheet 13



PROD TEST PATTERN

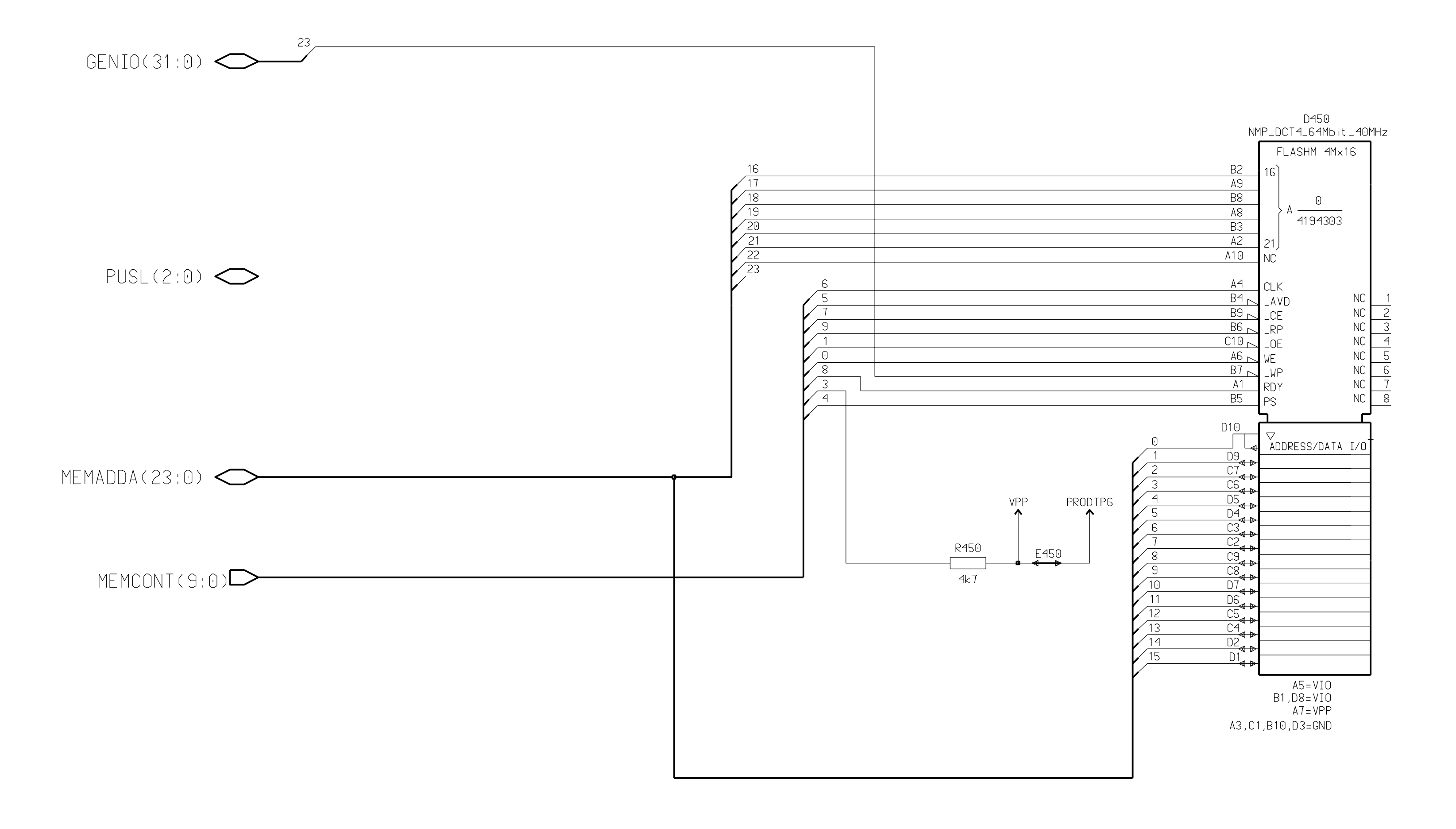
RF-BB Interface

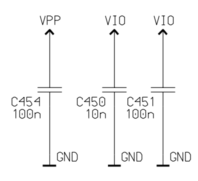


AMD 64 MBit

Sheet 15

Do not use this sheet with UPP version 1





MEMORY
(AMD 64 MBIT)

Test and Emulator Interface

Sheet 16



Sheet 17



Sheet 18

EMU

JTAG Emulator Connector and Buffers

Sheet 17



JTAG

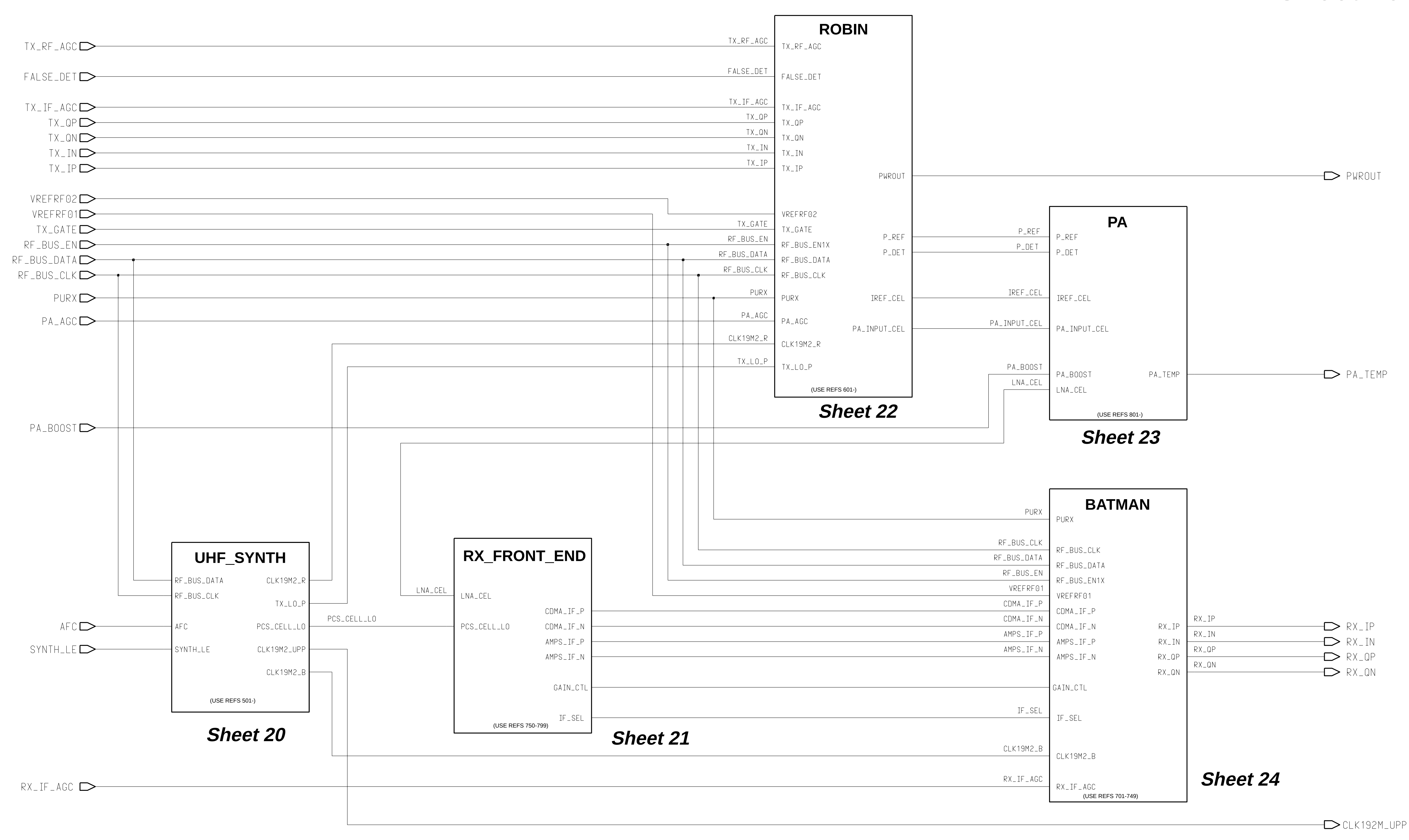
Connector-based Ostrich Test Interfacel

Sheet 18



OSTRICH

RF - Top Level


Sheet 19
ROBIN
PA
BATMAN
UHF_SYNTH
RX_FRONT_END
Sheet 20
Sheet 21
Sheet 22
Sheet 23
Sheet 24
TX_RF_AGC
FALSE_DET
TX_IF_AGC
TX_QP
TX_QN
TX_IN
TX_IP
VREFRF02
VREFRF01
TX_GATE
RF_BUS_EN
RF_BUS_DATA
RF_BUS_CLK
PURX
PA_AGC
PA_BOOST
AFC
SYNTH_LE
RX_IF_AGC
PWROUT
PA_TEMP
RX_IP
RX_IN
RX_QP
RX_QN
CLK192M_UPP
RF TOP

UHF Synthesizer

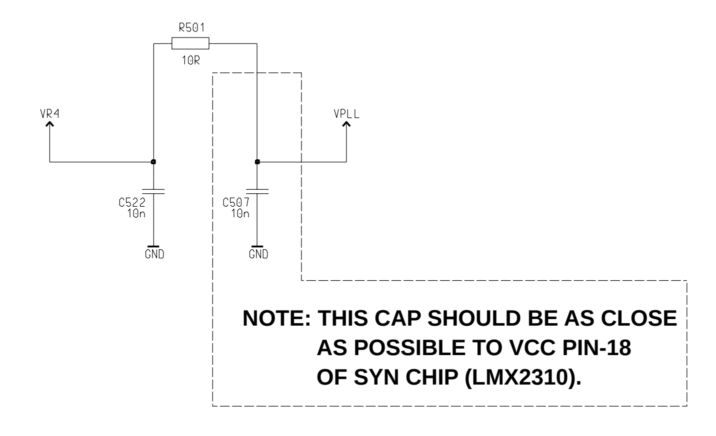
Sheet 20

KYOCERA 5 X 3.2 X 1.5mm
high pullability, high voltage VCTCXO

Initial time constant has been agreed with DSP
team to be 1.5ms (product of R511 and C503)

Remove this R for external UHF LO

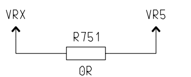
AFC
SYNTH_LE
RF_BUS_DATA
RF_BUS_CLK
CLK19M2_B
CLK19M2_R
CLK19M2_UPP
PCS_CELL_LO
TX_LO_P



UHF_SYNTH

RX Front End

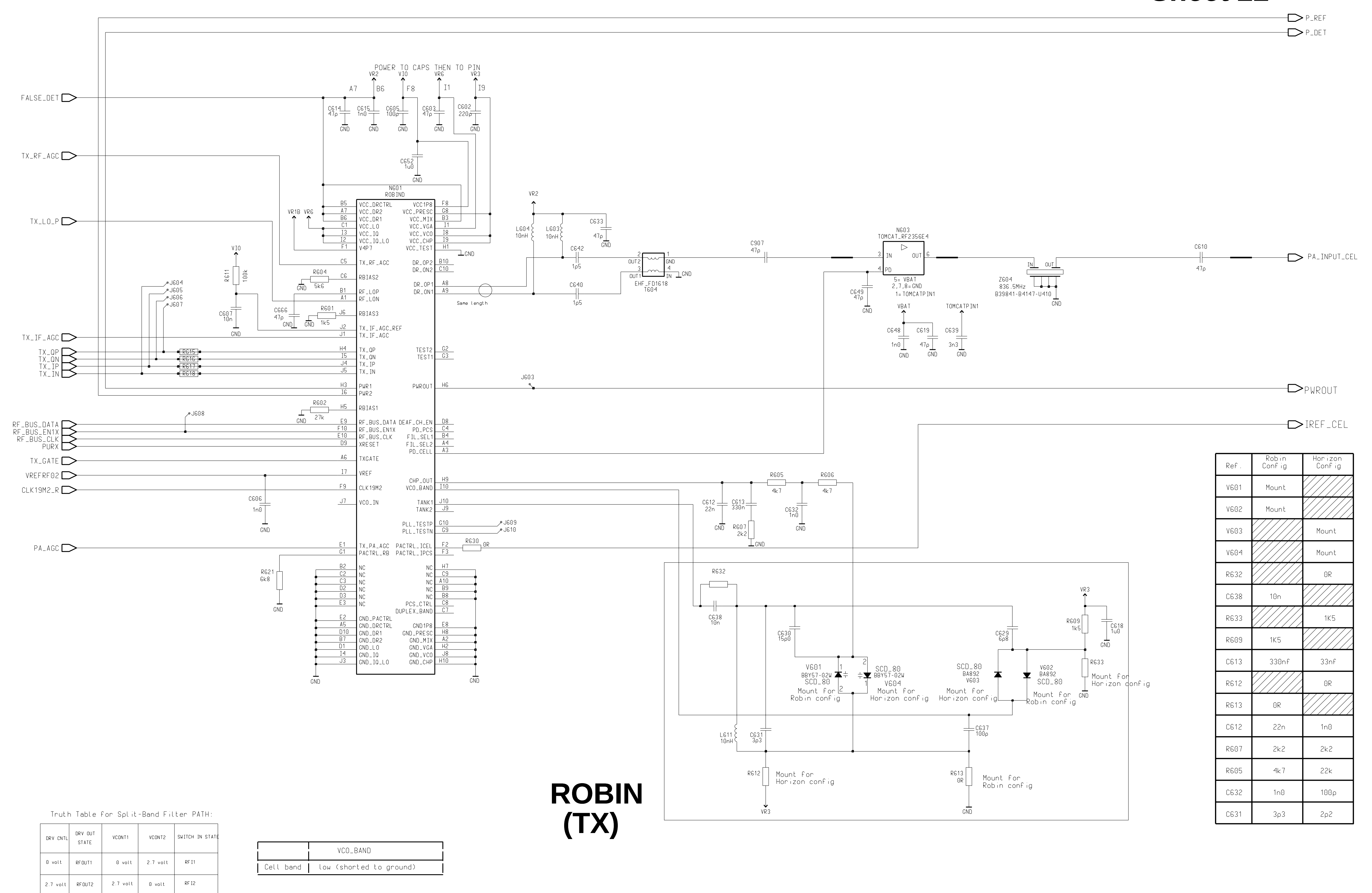
Sheet 21



	LOGIC INPUTS		
MODES	BAND	GAIN_CTL	IF_SEL
CEL CDMA Hi Gain	0	1	0
CEL CDMA Lo Gain	0	0	0
PCS CDMA Hi Gain	1	1	0
PCS CDMA Lo Gain	1	0	0
AMPS Hi Gain	0	1	1
AMPS Lo Gain	0	0	1

RX FRONT END

Robin TX



Ref.	Robin Config	Horizon Config
V601	Mount	
V602	Mount	
V603		Mount
V604		Mount
R632		0R
C638	10n	
R633		1K5
R609	1K5	
C613	330nF	33nF
R612		0R
R613	0R	
C612	22n	1n0
R607	2k2	2k2
R605	4k7	22k
C632	1n0	100p
C631	3p3	2p2

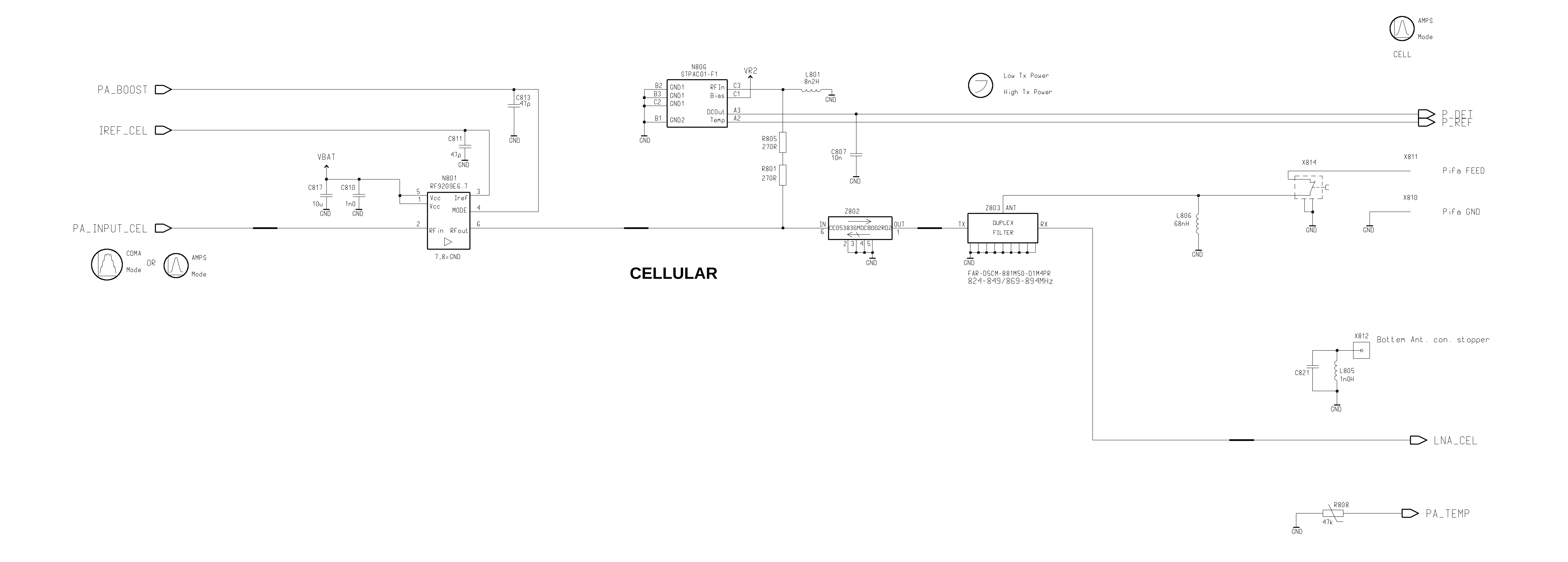
Truth Table for Split-Band Filter PATH:

DRV CNTL	DRV OUT STATE	VCONT1	VCONT2	SWITCH IN STATE
0 volt	RFOUT1	0 volt	2.7 volt	RFI1
2.7 volt	RFOUT2	2.7 volt	0 volt	RFI2

	VCO_BAND
Cell band	low (shorted to ground)

PA

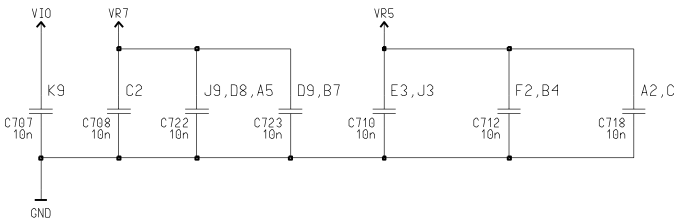
Sheet 23



PA

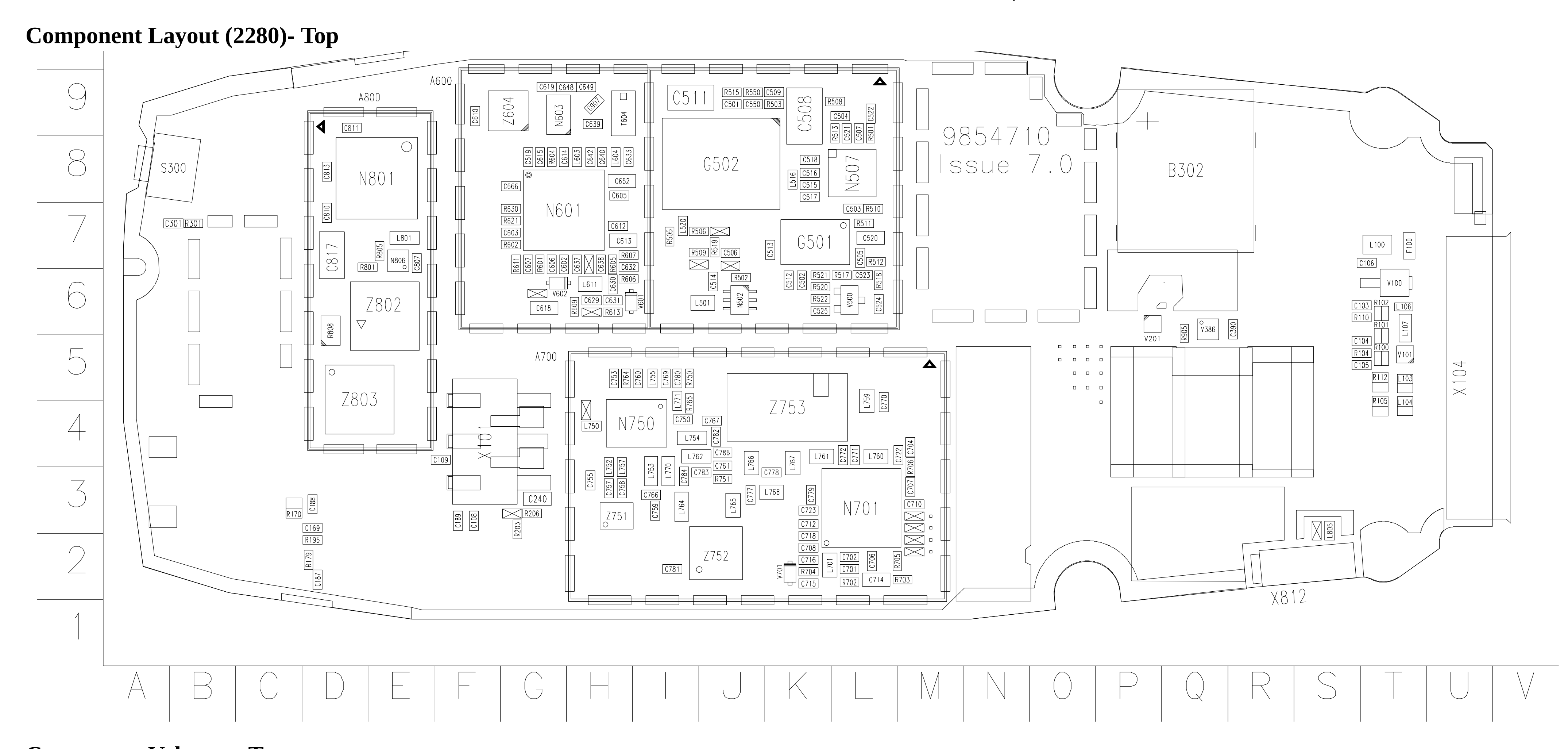
Batman RX

Sheet 24

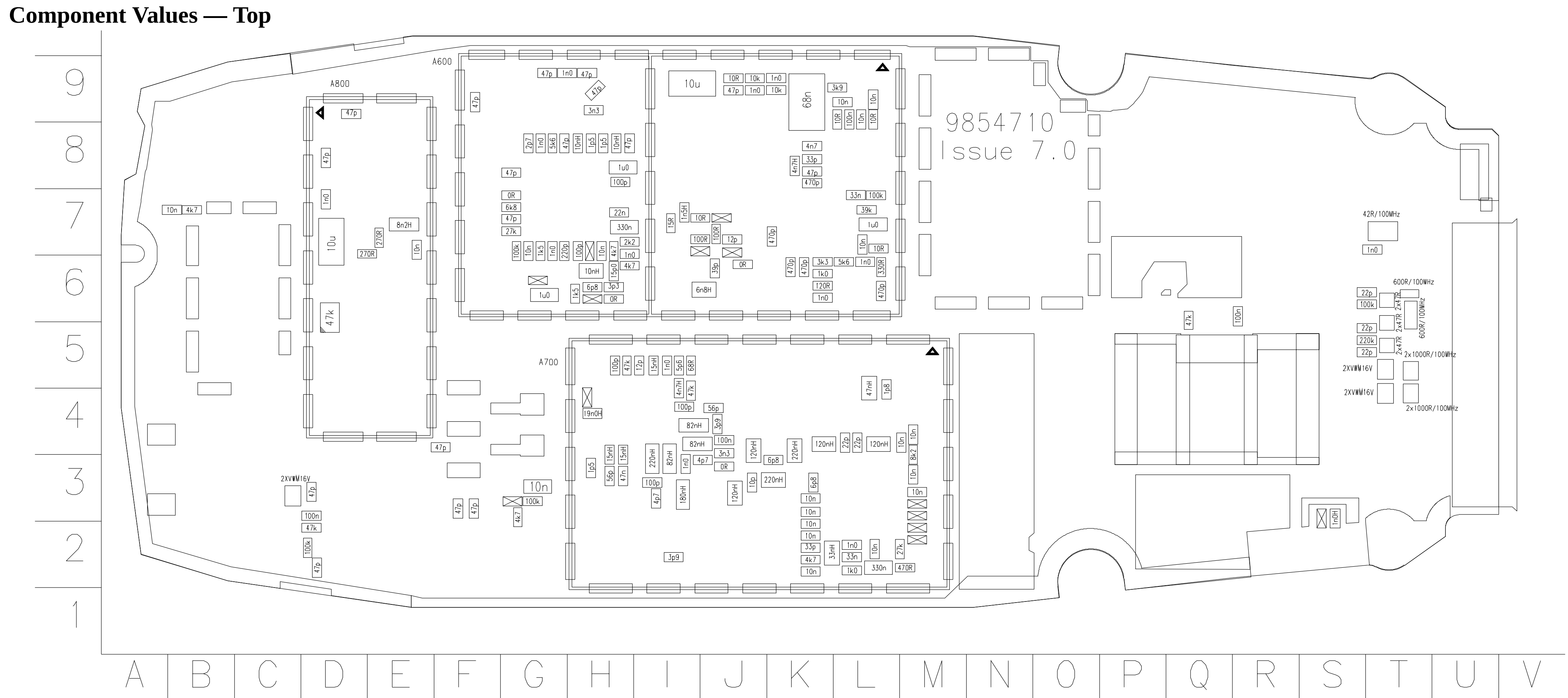


BATMAN (RX)

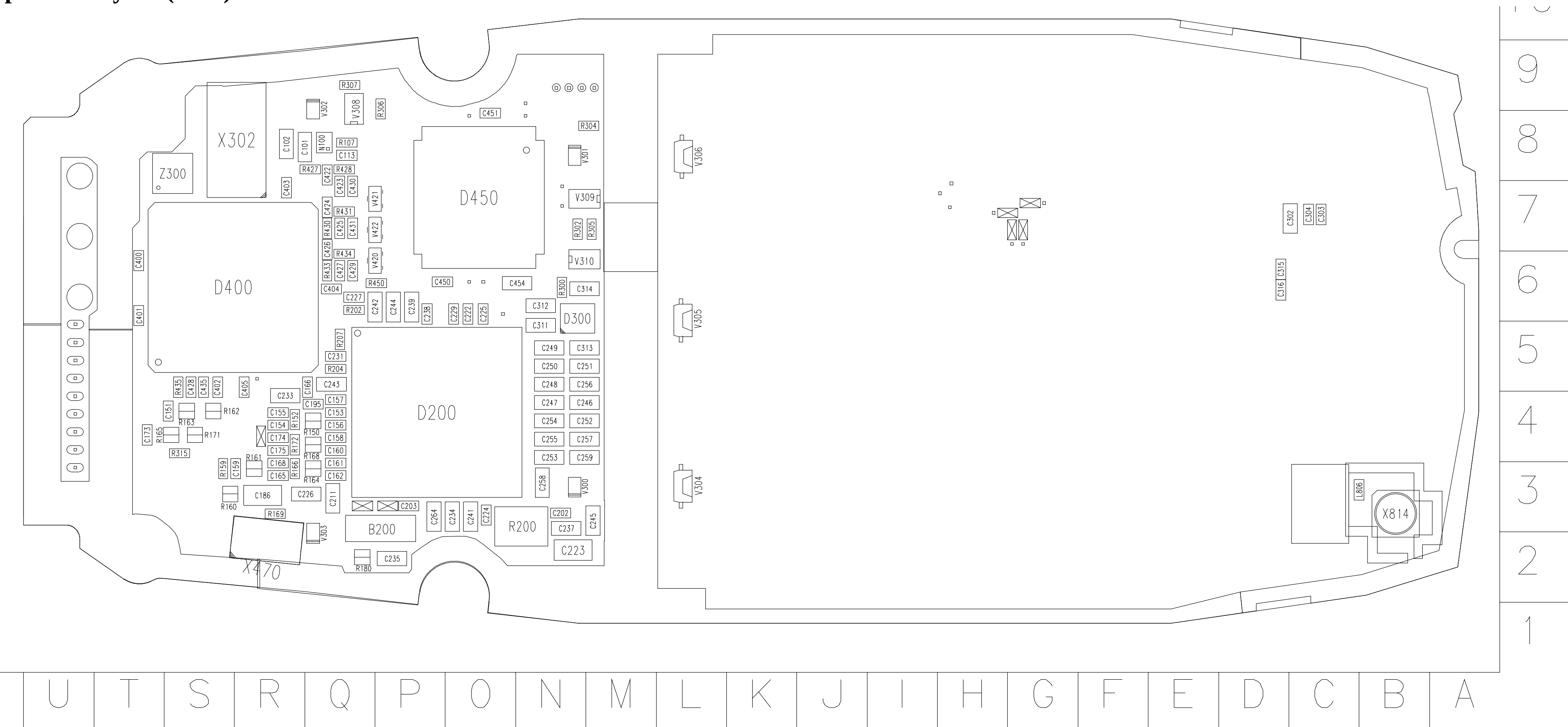
Component Layout (2280)- Top



Component Values — Top



Component Layout (2280) - Bottom



Component Values — Bottom

